PRÉCIS OF THE SEMICONDUCTOR INTEGRATED CIRCUIT LAYOUT DESIGN ACT, 2000

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ABSTRACT

The contemporary epoch is equipped with modern and advanced technology. The emergence of Information Technology, and the willingness of the States to be Hi-tech, has channelized the research into the field of electronics and communications. This has led to a new invention known as integrated circuits, which has volatilized the earlier technology. The aftermath of this was the emergence of a new intellectual property known as, *Semiconductor Integrated Circuit Layout Design.* To protect this new intellectual property, the Global leaders to safeguard their interest agreed to meet, and the *"Washington Treaty on Intellectual Property in Respect of Integrated Circuits, 1989"* was signed. The provisions of this treaty have been further incorporated in the TRIPs Agreement of the World Trade Organization (W.T.O) with some modifications.

This Current article is intended to analyze, the evolution and development, along with statutory protection available, with special reference to the Indian statute **"The Semiconductor Integrated Circuit Layout Design Act, 2000".**

***Keywords*:** Intellectual, Property, Rights, Semiconductor, Layout design, Integrated Circuits.

HISTORY AND EVOLUTION

Modern technology has started its journey in the year 1947 when at Bell Telephone Laboratories (U.S.A) *Bardeen* invented Transistors. Later on, when *Jack Kilby* (1958) and Robert Noyce (1959), when first devised the practical monolithic circuits[i], it has fashioned the new concept in the field of electronics. The U.S military was the first consumer of semiconductors integrated circuits[ii]. Since then, till today there is continuous upgrading in the field of semiconductors integrated circuits-based technology and in the modern era, it has established its roots throughout the globe.

In the inauguration age itself, Semiconductor integrated circuits technology has faced a clash regarding piracy. This clash was the cause of worry since there was no specific law to provide relief related to issues of piracy. Later on to control the chip piracy the industries approached the Copyright Office to get a solution to the issue but there also no remedy was granted to them.

The worry and concern for being protected have led the manufacturers, to protest to obtain Sui generis[iii] statute (of its kind or class), for semiconductor integrated circuit layout design based intellectual property, which shall provide relief to them from the issue of piracy. The aftermath of this protest was that *the United States Congress in 1984* has enacted the *Semiconductor Chip Protection Act (SCPA) 1984*[iv].

After the United States, various nations have also enacted the statute to grant protection for semiconductor integrated circuit layout design. But the National statutory protections have territorial limits. The aspect of global protection was first acknowledged in a multinational diplomatic conference known as *Washington Treaty on Intellectual Property in Respect of Integrated Circuits, 1989* which was held at Washington D.C., in 1989. The treaty was open for member states of the United Nations (U.N) and World Intellectual Property Organization (WIPO) including, some Intergovernmental Organizations meeting certain criteria. Afterward, it has been incorporated into the TRIP S Agreement of the World Trade Organization (WTO), with some modifications.[v] Under the TRIPS Agreement, the protection of layout design of integrated circuits at the global level was mentioned under Section 6, Article 35 to 38[vi].

Six years later to TRIPS Agreement, India has also ratified the obligation made under the TRIPS agreement and enacted the statute, named *"The Semiconductor Integrated Circuit Layout Design Act, 2000"* in the year 2000.

THE SEMICONDUCTOR INTEGRATED CIRCUIT LAYOUT DESIGN ACT, 2000: OVERVIEW

The Government of India, on the 4th of September, 2000, to ratify the TRIP S agreement, has enacted the *Semiconductor Integrated Circuits Layout-Designs Act, 2000*. The Act extends to the whole of India and was enacted to protect proprietor and users of the Semiconductor Integrated Circuit Layout Design and for the matters connected therewith or incidental thereto.

To fulfill International obligations, the Act, embodies the results of the Uruguay round of multi-trade negotiations done at Marrakesh on the 5th day of April 1994 and has also provided the establishment of the World Trade Organization.

The Act is constituted with ten (10) Chapters and ninety-six (96) Sections.

Key Definitions:

- **Section 2(h) "Layout-Design"-** layout-design means a layout of transistors and other circuitry elements and includes lead wires connecting such elements and expressed in any manner in a semiconductor integrated circuit.
- **Section 2(r) "Semiconductor Integrated Circuit"-** "semiconductor integrated circuit" means a product having transistors and other circuitry elements which are inseparably formed on a semiconductor material or an insulating material or inside the semiconductor material and designed to perform an electronic circuitry function.
- **Section 2(e) "commercial exploitation"-** "commercial exploitation", in relation to Semiconductor Integrated Circuits Layout-Design, means to sell, lease, offer or exhibit for sale or otherwise distribute such semiconductor integrated circuit for any commercial purpose.
- **Section 2(f) "convention country"-** "convention country" means a country notified as such under section 93;
- **Section 2(*l*) "register"-** "register" means the Register of Layout-Designs referred to in section 6;
- **Section 2(m) "registered"-** "registered" (with its grammatical variations) means registered under this Act;

REGISTRAR: APPOINTMENT AND POWER

For this Act, the Registrar and other such officers who work following the direction given by Registrar was appointed by the Central government[vii]. The notice of appointment shall be published by the Central Government in the official gazette. With the notification published in the official gazette dated 1st March 2004, *Dr. K.S. Chari,* who was Scientist G, in the department of Information technology, was appointed to hold additional charge of Registrar of Semiconductor Integrated Circuits Layout-Design[viii].

The duly appointed registrar is vested with certain powers- one such power is that he can transfer any matter pending before any officer of his office and such matter thereafter can be dealt either by registrar himself or he may transfer the same to another officer, whereby the proceedings may be *de novo* or from the stage when it was withdrawn[ix].

The Registrar while exercising his powers may withdraw the given acceptance (before the registration) to such applications, which were under the obligation of section 7 of the Act. Before withdrawal, a notice has to serve to the applicant and in the prescribed time the applicant shall be allowed to be heard.[x]

If any registered user is performing an *ultra vires* act with respect to a contract created between the Registered Proprietor and him, then over the application made to the Registrar, Registrar has the power to cancel the registration of such registered user. Other than this if any misrepresentation, or failure to disclose the material facts, or changes occur in circumstances and due to which the registration of the registered user cannot be justified then The registrar has to issue a notice to such registered proprietor and registered user in prescribed manner with the reasonable opportunity to be heard and after that Registrar can cancel the registration of the registered user.[xi] The Registrar has also the power to rectify the record i.e. Register[xii].

Further in all the proceedings under Semiconductor Integrated Circuit Layout Design Act, 2000, Registrar has all the power of civil courts for the purpose such as receiving evidence, administering oaths, enforcing the attendance of witnesses, etc. and over an application made in the prescribed manner may review his own decision.[xiii]

REGISTRY OFFICE AND REGISTER

In Exercise of the Power conferred the central Government established a registry which shall be known as Semiconductor Integrated Circuit Layout Design Registry and in order to such Central Government has published the notification in official gazette that the head office of the Semiconductor Integrated Circuit Layout-Design Registry so established shall be located in the department of Information Technology, C.G.O. Complex, Lodhi Road, New Delhi whose territorial limit within which such office of the Semiconductor Integrated Circuit Layout Design registry may exercise its functions shall be whole of India[xiv].

There shall be a register in which all the essential entries of the registered layout designs are to be entered in a prescribed manner and it shall be placed at the head office of the Semiconductor Integrated Circuits Layout-Design Registry, under the control and management of the Registrar. The copy of this register shall be kept at each Branch office of the Semiconductor Integrated Circuits Layout-Design Registry.[xv]

APPLICATION OF REGISTRATION, PROCEDURE, REGISTRATION AND DURATION

Any person who is a creator and having the desire to register his integrated circuit layout design shall write in a prescribed manner to the registrar and such application shall be filed at such registry office under whose jurisdiction the principal place of business of applicant is situated. When the application is made by joint creators then in such cases the registry office will be according to the business place of first applicant. If business is not carried in India than in such situations the application shall be filed in that office under whose territorial limit the applicant is providing services, as mentioned in the application of registration.[xvi]

All the application which comes to the registrar then over such application, registrar may either accept them *per se* else if certain modifications are needed then he may ask the applicant for the same. If registrar rejects the application over any grounds provided by the act he shall notify the applicant for the same and after giving the chance to be heard, if not satisfied with the applicants reply he may reject the application. Registrar can withdraw any acceptance which is

given to any application for registration but prior to registration[xvii], registration if the material to be registered falls under such layout designs which are been prohibited for registration.[xviii]

The post acceptance procedure is that within fourteen days of acceptance the acceptance shall be published in a prescribed manner[xix]. After publishing if any person goes up against such application then he shall in a written and prescribed manner long with prescribed fee for such application, can file the application to the registrar. Thereafter registrar shall notify the applicant along with the copy of application raising opposition. Over which within the two month from date of receiving the notice the applicant has to file up his counterstatement, and this counterstatement shall be again notified to the opposing applicant.

If there is any evidence available to any applicant, such shall be submitted to the registrar in a prescribed manner, subsequently after going through the evidence and hearing both the parties' registrar may allow or decline the application of either party[xx].

When an application made for registration qualifies the registration process, subsequently Registrar shall grant to the applicant with the certificate of registration having seal of registry over such certificate.[xxi] In case where there are two or more than two creator of layout design and their jointly effort cannot be distinguishable in creation of that layout design then the registration made will be joint registration.[xxii]

The registration of a layout design shall be only for a period of ***ten years*** which shall be Counted from the date of filing a application for registration or From the date of first commercial exploitation anywhere in any country whichever is earlier[xxiii]

EFFECT OF REGISTRATION

Registered layout designs operate as a prima facie evidence in all the legal proceedings made under semiconductor integrated circuit lay out design Act, 2000[xxiv], other than this no person shall be entitled to institute any proceedings to prevent or to recover any damages for, the infringement of an unregistered layout design[xxv].

RIGHTS CONFERRED

Once the certificate of registration has been issued to the proprietor, he has the exclusive rights to use the layout design and also, he can obtain relief in case of infringement of his rights.[xxvi] The registered proprietor has also vested with the power of assignment and transmission when the proprietor assigns the layout design to other person, he has to issue effectual receipts for any consideration over such agreements[xxvii].

INFRINGEMENT OF LAYOUT DESIGN

Any person other than registered proprietor and registered user, when knowingly and willfully does any act of reproducing whether by incorporating in a semiconductor integrated circuit or in any part of registered design. It will constitute to infringement. But for certain purpose like scientific evaluation, analysis and research or for the purpose of teaching, such acts does not mount to infringement[xxviii]. Along with this all other ground mentioned in the Act, will constitute infringement.

APPELLATE BOARD

An appellate board is constituted by the Central Government which exercises jurisdiction, powers and authority conferred on it by the Semiconductor Integrated Circuit Layout Design Act, 2000[xxix]. When a decision is delivered by the appellate board if the party to decision is not satisfied with such decision in a prescribed period they may approach to High court having jurisdiction to consider such matter[xxx].

OFFENCES, PENALTIES AND PROCEDURE

If any person knowingly and willing fully causes infringement under section 18 of the Act, he shall be punished with imprisonment for a term which may extend to three years or with fine which shall not be less than fifty thousand rupees but which may extend to ten lakh rupees, or

both[xxxi] along with this several other penalties are mentioned in chapter IX of the Semiconductor Integrated Circuit Layout Design Act, 2000.

CONCLUSION

The Semiconductor Integrated Circuit Layout Design Act, 2000, is an extension and ratification of International Agreements to whom India is a signatory. The statute provides a comprehensive protection to the semiconductor integrated circuit layout designs and recognized it as an Intellectual Property. It helps the intellects since their interest and work is being protected and a bundle of rights are also granted to them statutorily. Other than proprietors, it will also encourage the number of Indian companies who are willing to establish themselves in the business of integrated circuit layout design.

ENDNOTES

[i] Richard N. Langlois and W. Edward Steinmueller, The Evolution of Competitive Advantage in the Worldwide Semiconductor Industry, Chapter 2 p. 31 (1947-1996).
[ii] Id. at 23.
[iii] Leon Radomsky, Sixteen Years After the Passage of The U.S. Semiconductor Chip Protection Act: Is International Protection Working? Berkeley Technology Law Journal 1052 [Vol. 15:1049].
[iv] Id. at 1056.
[v] Available at https://en.wikipedia.org/wiki/Integrated_circuit_layout_design_protection visited on 30 September 2019.
[vi] Available at https://www.wto.org/english/docs_e/legal_e/27-trips.pdf visited on 30 September 2019.
[vii] Semiconductor Integrated Circuit Layout Design Act, 37 of 2000, Section 3
[viii] The Gazette of India, Extraordinary, Part II, Section 3- Subsection (ii), S.O. 277 (E)., dated 1st March 2004
[ix] Id. Section 4
[x] Id. Section 9
[xi] Id. Section 26
[xii] Id. Section 30
[xiii] Id. Section 72
[xiv] The Gazette of India, Extraordinary, Part II, Section 3- Subsection (ii), S.O. 279 (E)., dated 1st March 2004.
[xv] Semiconductor Integrated Circuit Layout Design Act, 37 of 2000, Section 6
[xvi] Semiconductor Integrated Circuit Layout Design Act, 37 of 2000, Section 8
[xvii] Id. Section 9
[xviii] Id. Section 7
[xix] Id. Section 10
[xx] Id. Section 11
[xxi] Id. Section 13
[xxii] Id. Section 14
[xxiii] Id. Section 15
[xxiv] Id. Section 19
[xxv] Id. Section 16

[xxvi] Id. Section 17
[xxvii] Id. Section 20-22.
[xxviii] Id. Section 18
[xxix] Id. Section 32
[xxx] Id. Section 53
[xxxi] Id. Section 56